Benefits of Embedded RAM in FLEX 10K Devices

Introduction

Driven by the demand to integrate many more digital functions in a single device, custom logic devices are growing in density as fast as process technology will allow. Today, most gate array densities range from 50,000 to 100,000 gates, although densities above 400,000 gates are not uncommon.

Although gate array densities have increased, the broad categories of digital building blocks have not changed. Typically, the building blocks consist of specialized core logic functions such as microcontrollers or digital signal processing (DSP) functions, both of which include RAM and general interface logic. The complexity and capability of these blocks have grown with device density, but core logic and DSP are still considered the fundamental building blocks of most digital systems.

Historically, programmable logic devices (PLDs) have addressed general logic requirements, but have not successfully addressed the requirements for RAM and core logic building blocks. PLDs have not been effective in providing the densities necessary to implement large, specialized logic functions and have not provided the RAM capabilities that digital systems require. Thus, PLDs that can address these needs are an effective alternative to programming with gate arrays.

Altera's FLEX 10K device family introduces to the industry the first PLDs with embedded memory for RAM and a logic density of over 60,000 gates. FLEX 10K devices can integrate complex logic cores, RAM, and general interface logic—all in one standard, off-the-shelf device.

EAB Architecture

Every FLEX 10K device contains several embedded array blocks (EABs) with a DATA bus of variable width (8, 4, 2, 1) and an ADDRESS bus of variable width (11, 10, 9, 8). Unlike distributed RAM in FPGAs, the FLEX 10K EAB is designed to ensure predictable, easy-to-use timing. The EAB Write Enable (WE) signal can be synchronized with the input Clock, or can be asynchronous. The EAB also contains input, output, and address registers that synchronize a design. EAB outputs can be registered or combinatorial. Registered outputs provide a higher operating frequency than combinatorial outputs. Figure 1 shows the EAB block diagram.

*Figure 1. EAB Block Diagram*
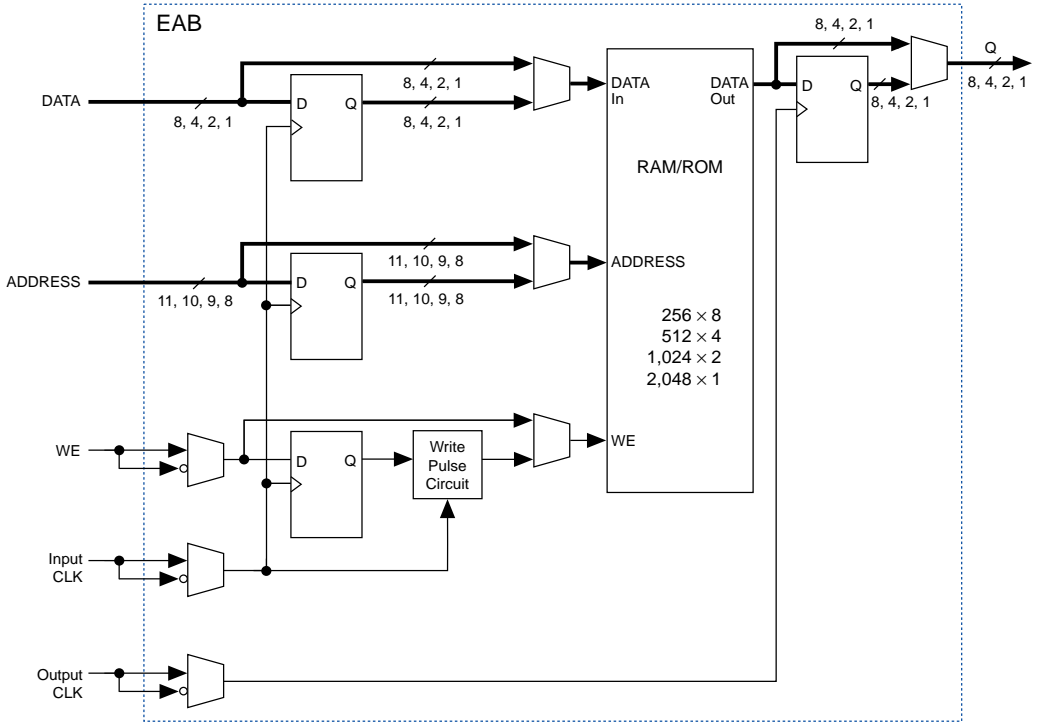
Using EABs

The EAB RAM size is flexible; therefore, you are not limited to one RAM configuration such as 2,048 words of 1 bit each. The following RAM sizes are available:

- 256×8
- 512×4
- $1,024 \times 2$
- $2,048 \times 1$

The width of the DATA and ADDRESS buses varies with the size of the RAM. You can configure an EAB for any size with standard EDA tools or with Altera's MAX+PLUS II development system. Figure 2 shows a graphical representation of the flexible RAM sizes.

Figure 2. EAB Memory Configurations

| 256 × 8 | 512 × 4 | 1,024 × 2 | 2,048 × 1 |
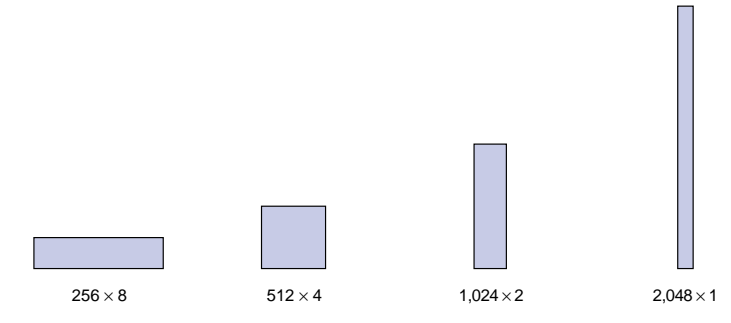
Embedded vs. Distributed RAM

Most field-programmable gate arrays (FPGAs) distribute RAM, allowing the user to choose how a particular array of memory cells will be utilized—for example, as part of the general logic array or as addressable RAM. However, using distributed memory in applications requiring RAM blocks larger than 32×1 results in lower performance and lower device utilization in FPGAs.

In contrast, FLEX 10K devices feature embedded RAM, and with embedded RAM, an area of the device is dedicated to memory cells so that the overhead structures required for RAM—addressing and write control—are very fast and efficient. Thus, the largest FLEX 10K device offers 24 Kbits of RAM without sacrificing logic capacity.

Figure 3 shows how the available logic of an FPGA varies with the amount of RAM implemented in the device. Implementing RAM in FPGAs reduces available logic, whereas implementing RAM in FLEX 10K devices does not affect the logic capacity. As RAM sizes increase, the logic capacity of an FPGA decreases because more logic is required to generate the multipliers that combine small RAM blocks. As a result, the entire device cannot be configured as RAM.

True system-level integration of complex digital designs requires integrating RAM in addition to logic. The integration capabilities of FPGAs are limited because they lose logic capacity when RAM is used. According to calculations by Altera Applications, a block of RAM as small as 12 Kbits consumes about 50% of the logic capacity of a Xilinx XC4025E. In contrast, FLEX 10K devices have dedicated embedded RAM for applications that require larger RAM configurations, which can be used without impacting the logic capacity of the device.

Figure 3. RAM vs. Logic Tradeoff
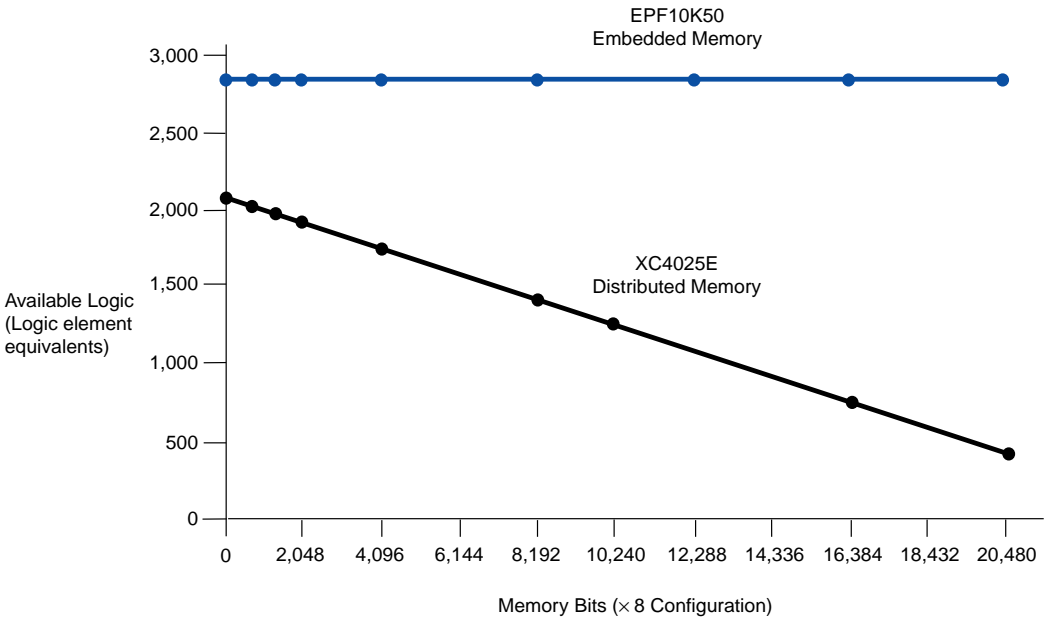
Source: Altera Applications

Efficiency of Embedded RAM

The FLEX 10K embedded RAM is more efficient than distributed RAM because of its size and implementation. The size of a fundamental FPGA RAM block is limited by its logic architecture: an n-input look-up table (LUT) can contribute only 2^n bits. Therefore, large RAM blocks must be built from very small blocks of RAM. To combine small RAM blocks, extra logic cells must generate wide address decoders for writing to the RAM and address multiplexers for reading the RAM. These extra logic cells must be used to implement large RAM blocks even though they do not directly contribute to the RAM size.

A high percentage of the die area required to implement RAM in an FPGA contributes to overhead, not RAM bits. Therefore, the FPGA architecture forces inefficiencies in RAM implementations. In fact, a RAM block with a depth of 256 words requires approximately 10 times more die area than the same RAM block implemented in a FLEX 10K device. The inefficiency of FPGAs directly translates into a higher cost per bit of RAM.

In contrast, the RAM implemented in FLEX 10K devices is dedicated as RAM. Because FLEX 10K RAM is dedicated, it is optimized for die area and performance, and provides all the benefits of embedded RAM. These factors make FLEX 10K embedded RAM the most efficient RAM in the programmable logic market today.

For any given RAM size, embedded RAM is much more efficient than distributed RAM. Figure 4 compares the relative die areas of common RAM sizes.

Figure 4. RAM Efficiency
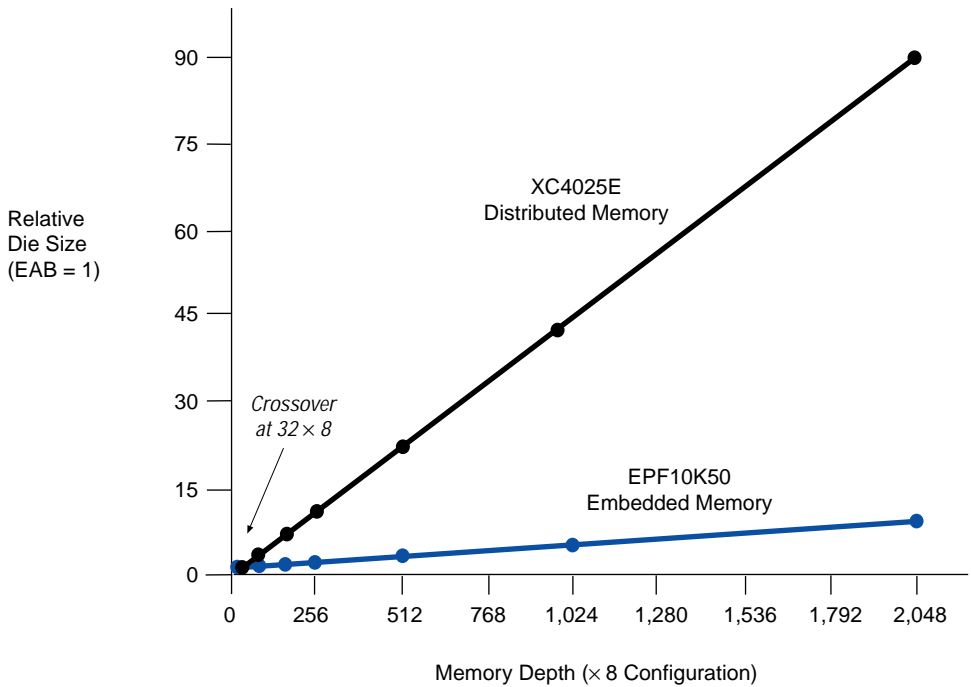
Source: Altera Applications

RAM Performance

The length of the cycle time is a good indicator of RAM performance. Writing to RAM involves presenting data and an address, and then generating a write pulse to store the data in the appropriate memory location. In FLEX 10K devices, all of the supporting circuitry for embedded RAM is built directly into the die. Required die area is reduced, and building the supporting circuitry into the die provides faster, more predictable performance.

As RAM depth increases, the cycle time for an FPGA increases because more support logic is required. In contrast, the cycle time for a FLEX 10K device remains constant at various RAM depths because the FLEX 10K embedded array block (EAB) has a higher logic capacity. Figure 5 compares cycle performance versus memory size for the Xilinx XC4025E and the Altera EPF10K50 devices.

Figure 5. Cycle Time
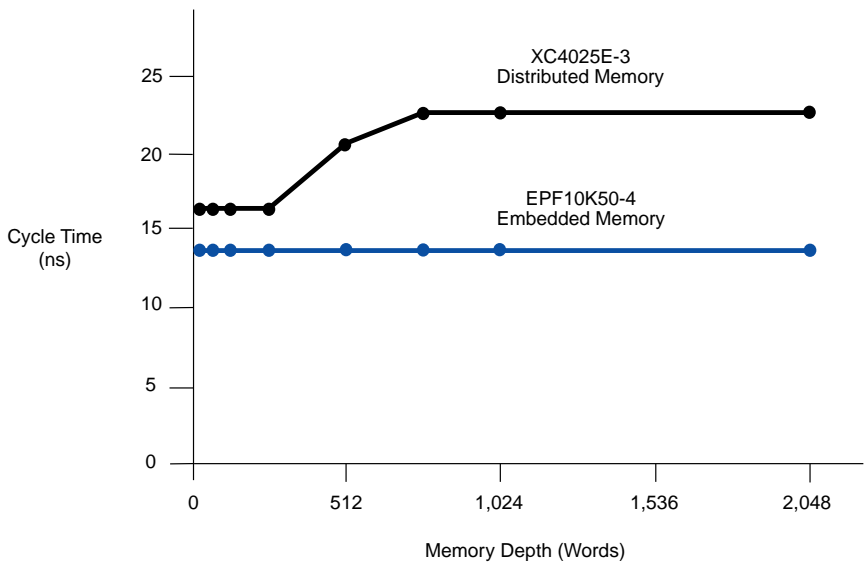
Source: Altera Applications

Cascading EABs for Wider RAM

For designs requiring blocks of RAM wider than an EAB configuration, the MAX+PLUS II software automatically cascades EABs to implement larger blocks of RAM. See Figure 6. Because cascading FLEX 10K EABs does not require additional logic, they have the same 13.8-ns cycle time as non-cascaded EABs.

Figure 6. Cascaded EABs
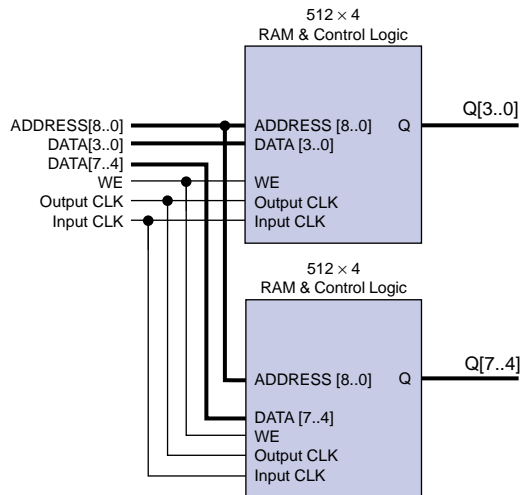
Unlike FLEX 10K EABs, distributed RAM in FPGAs only has predictable access times for small, individual RAM blocks, such as 32×1. As the size of the FPGA RAM increases, additional RAM blocks are needed, and the access times become significantly slower. For example, a 256×8 RAM block in a typical FPGA may require a 15.8-ns cycle time and use a significant number of device resources in addition to RAM.

Synchronous RAM

To use a FLEX 10K EAB for synchronous RAM, the DATA and ADDRESS signals should be registered. All control signal timing, including the WE signal, is implemented in the EAB. Generating the WE signal with the EAB eliminates potential glitches that can corrupt data. When a high WE signal is clocked into the EAB, circuitry inside the EAB generates a write pulse that meets setup and hold times for the DATA and ADDRESS inputs. You do not have to de-assert WE to

write on consecutive Clock cycles because the synchronous EAB allows ADDRESS inputs to change while WE is high. The WE signal automatically pulses high on each Clock cycle.

Asynchronous RAM

You can configure the FLEX 10K EAB for asynchronous RAM using the following guidelines:

- The WE signal must be timed to avoid glitches that can unintentionally overwrite the RAM.
- The WE signal must meet the setup and hold times for the DATA and ADDRESS inputs and signals.
- The ADDRESS inputs cannot be changed while WE is high.

Conclusion

The die area efficiency and performance capabilities of embedded RAM make it superior to distributed RAM. Embedded RAM is easy to use, provides predictable timing and flexible configurations, and creates implementations that are fast enough to fit a wide variety of applications with complex logic functions. FLEX 10K devices are the first high-density PLDs that are a suitable alternative to designs typically implemented in gate arrays.

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